REMARKS

Claims 1-17 have been presented in the above-identified U.S. Patent Application.

Claim 5, 6, and 11-13 have been withdrawn as being directed to non-elected subject matter.

Claim 1, 3, 4, 7, 8, 14 and 15 have been amended by this Amendment A.

Claim 2 has been cancelled.

Claims 1, 3, 4, 7-10, and 14-17 are in the Application and reconsideration of the Application is hereby respectfully requested.

Referring to Page 2 of the Office Action, Claims 5, 6, and 11-13 have been withdrawn without traverse by Applicant's attorney. As indicated in Paragraph 1 of the Office Action, Claims 1-4, 7-10, and 14-17 remain in the Application.

Referring to Paragraph 4 of the Office Action, the Drawings have been objected to. Transmitted herewith are Replacement Drawings including the labeling of Fig. 1 as PRIOR ART.

Referring to Paragraph 5, Claims 1, 7, and 14 have been objected to because of Claim informalities kindly

pointed out by Examiner. The cited informalities have been corrected by this Amendment A. Therefore, objection to Claims 1, 7, and 14 because of the cited informalities has been answered by amendment.

Referring to Paragraph 6 of the office Action, Claims 2, 4, and 8 have been rejected under 35 U.S.C. 112, second paragraph because of cited ambiguities. By this Amendment A, the cited ambiguities have been corrected. Therefore, rejection of Claims 2, 4, and 8 under 35 U.S.C 112, second paragraph, has been answered by amendment.

Referring to Paragraph 7 of the Office Action, Claims 1-4, 7-10 and 14-17 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. PN: 5,490,155 issued in the name of Abdoo et al, here-in-after referred to as Abdoo. The Abdoo reference is essentially an elaborate description of Fig. 1, i.e., the prior art. For example, on Page 10 of the Office Action, Examiner states "an interrupt request (IRQ) signal indicating that a correctable error has occurred (see col.11, lines 62-67)." This quotation refers to a correctable error in a signal group that is detected by the error checking and correction unit and can be corrected by the well known methods of the error checking and correction techniques, a prior art capability. In contradistinction, the present invention relates to the correction of the storage element itself in which the error signal is generated by reason of a failing bit. Note that there are a variety of failing bits memory locations in the prior art. The present disclosure

discusses only failing bit locations in non-volatile memory locations. These types of failing bit locations can be corrected by altering the physical properties, e.g. as flash memory locations.

Referring to Claim 1, an independent Claim of the Application, (and Claims 3 and 4 depending there from), Claim 1 has been amended to be consistent with the disclosure found in the description of Specification. In particular, the amendments to Claim 1 emphasize that a correctable location in the memory itself, has been identified and can be correctable. Referring to the Summary of the Invention, "When the central processing unit can be interrupted, the central processing unit restores the location in main memory where the error originated based on the stored address and location." Thus, the amendments to Claim 1 emphasize the invention that is sought to be protected. Without these amendments, the ambiguity exists that what is being described is the correction of an error in the signal group instead of the correction of the memory location storing the signal bit and generating the identified error. If the correction of a signal was meant, then the Claim, as filed would read on the prior art as described in the section of the application entitled Description of the Prior Art. In addition, the dependent Claims 3 and 4 make sense only in terms of the disclosure in the Specification regarding the correction of a failing bit memory location. Therefore, rejection of Claims 1, 3, and 4 under 35 U.S.C. 102(b) as being anticipated by Abdoo is respectfully traversed.

Referring to Claim 7, an independent Claim of the Application (and Claims 8-19 depending there from), this Claim has been amended, once again, to avoid ambiguity in the language that might confuse correction of a bit in a group of signals retrieved from a memory unit with the correction of a failing memory location causing the error signal. The inclusion of "location" in Claim 7 is a reflection of the use of the term "memory location" in dependent Claim 8. Referring to dependent Claim 9, the description found therein is understandable only in terms of the correction of non-volatile memory units. The description of the Claims in terms of the Abdoo reference is interpreting the Claims in view of the prior art described in the Application. The Abdoo reference nowhere describes the restoration of a memory cell once the memory cell has failed. Consequently, rejection of Claims 7-10 under 35 U.S.C. 102(b) as being anticipated by Abdoo is respectfully traversed.

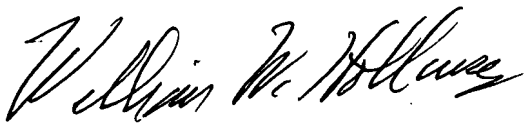
Referring to Claim 14 (and Claims 15-17 depending there from), claim 14 describes, inter alia, "the error apparatus generating a restore signal when the error is consistent with a failing bit location" and "a flag apparatus storing the associated correction pattern and the associated address in response to the restore signal". These limitations can be understood only when read in the context of the Specification. The context of the Specification clearly indicates that the correction pattern and the restore signal relate to the restoration of a failing bit memory location and not to the prior art

technique of error checking and correction wherein only an erroneous signal in a signal group is changed, the memory location is not affected. Claim 15, as amended, specifically refers to the correction of a memory location. Claim 16 specifically refers to the technique for correcting a non-volatile memory location described in the Specification. Thus, Claim 14 and Claims dependent there from are believed to protect a different invention from the invention described by the Abdoo reference, a reference which discloses the prior art technology of the volatile memory. Therefore, rejection of Claims 14-17 under 35 U.S.C. 102(b) over Abdoo is respectfully traversed.

CONCLUSION

In view of the foregoing discussion and the foregoing amendments, it is believed that Claims 1, 3, 4, 7-10, and 14-17 are now in condition for allowance and allowance of Claims 1, 3, 4, 7-10, and 14-17 is respectfully requested. Applicant(s) hereby respectfully request a timely Notice of Allowance be issued for this Application.

Respectfully submitted,



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